AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0005] with the following amended text:

Fig.1 is a schematic cross-sectional diagram showing a prior art PMOS transistor 10 having ultra-shallow junction S/D extensions 32. The prior art PMOS transistor 10 includes a poly gate 12 formed on an N well 16 of a silicon substrate. A gate oxide layer 14 is formed between the gate 12 and the silicon substrate. Spacers 18 are disposed on opposite sidewalls of the gate 12. A P^- ultra-shallow junction S/D extension 32 is formed underneath the spacer 18 within the N well 16. Next to the outer edge of the spacer 18, a raised silicide layer 42 is provided on P^+ source/drain region 34. A silicide layer 44 is formed on the top of the poly gate 12. Typically, the spacer 18 consists of an offset oxide spacer 21 stuck to the sidewall of the poly gate 12, an oxide liner 22, and a nitride spacer ~~22~~ 23. As specifically indicated in this figure, the oxide liner 22 covers the offset oxide spacer 21 and its lower portion extends laterally to directly cover and borders the P^- ultra-shallow junction S/D extension 32.

Please replace the paragraph [0022] beginning at page 6, with the following amended paragraph:

Still referring to Fig.4, the PMOS transistor 10 further comprises a raised cobalt silicide layer 42 formed on P^+ S/D region 34 next to the outer edge of the spacer 18. The cobalt silicide layer 42 may be formed by using a known selective epitaxial growth (SEG), followed by a self-aligned silicide

(salicide) process. A silicide layer 44 is formed on the top of the poly gate 12. The spacer 18 consists of an offset oxide spacer 21 stuck to the sidewall of the poly gate 12, an oxide liner 22, and a nitride spacer ~~22~~ 23. The oxide liner 22 covers the offset oxide spacer 21 and its lower portion extends laterally to overlie the SiGe epitaxial layer 60. In accordance with the preferred embodiment of the present invention, the SiGe epitaxial layer 60 is only formed on the P^- ultra-shallow junction S/D extension region 32. To prevent germanium of the epitaxial layer 60 from affecting the cobalt salcide process carried out on the S/D diffusion regions 34, the epitaxial layer 60 formed on the S/D diffusion regions 34 is completely removed.

Please replace the paragraph [0027] beginning at page 11, with the following amended paragraph:

As shown in Fig.9, the silicon nitride layer 23a and the liner 22a are anisotropically etched back to form spacers 18. The spacer 18 consists of the offset oxide spacer 21, the oxide liner 22, and the nitride spacer ~~22~~ 23. The oxide liner 22 covers the offset oxide spacer 21 and its lower portion extends laterally to overlie the SiGe epitaxial layer 60.